Abstract

Certain embodiments of the present invention relate to a semiconductor device that has a pad section having an excellent coherency with an interlayer dielectric layer, and a method for manufacturing the same. A semiconductor device 1000 has a pad layer 30A formed over an interlayer dielectric layer 20. The interlayer dielectric layer 20 includes at least a first silicon oxide layer 20b that is formed by a polycondensation reaction of a silicon compound and hydrogen peroxide, and a second silicon oxide layer 20c formed over the first silicon oxide layer and containing an impurity. The pad section 30A includes a wetting layer 32, an alloy layer 34 and a metal wiring layer 37.